

**In the Specification**

**Amend the specification as follows:**

**Amend the paragraph beginning at page 7 line 24 as follows:**

The present invention has direct application to center bus memory chips, although it may not be limited strictly to these types of devices. In a center bus memory device, the ~~bonds~~bond wires attach to the center of the chip. The chip is then bonded face down to the substrate, with electrical connections maintained through an aperture or window in the substrate. In this case, the bond wires attach to the opposite side of the substrate from that which the chip is bonded. In a two-chip offset stacked configuration, the lower chip may bond to the substrate through an aperture, as does the conventional single chip device. The upper chip is mounted to the backside of the lower chip offset in a single axis, such that the center wire bond bus is exposed. Electrical connection of the upper chip is by bonding to the edge of the lower chip substrate. Most circuits on the lower chip substrate are shared in common by both chips. Addresses and data lines are common. Controls may be may be separate depending upon the stacked electrical configuration. Circuitry and solder balls on the lower device substrate are used to interconnect both chips in the stack with the next level of assembly. The assembled dual chip stack is covered by an encapsulating resin enclosing a portion of the surfaces or all surfaces and wirebonds, save the bondable surface of the substrate.

**Amend the paragraph beginning at page 8 line 11 as follows:**

Importantly, the center bus chips are stacked with an offset in a single direction. The top layer of chips is wire bonded to the opposite side of the module substrate. The center bus is made to traverse to the substrate between two devices on the lower layer. To assemble the offset stacking

devices into a high density module, devices are placed sequentially on a module substrate such that approximately one half of the protruding lower memory device is used as a support for the overhanging upper memory device chip of the next device stack. Fig. 2A is a partial schematic of a double density stack assembly of the present invention. A dual in-line memory module (DIMM) substrate 200 supports multiple layers of device memory chips. A discrete device or spacer 202 begins the lower layer assembly having connections to the substrate via ball grid arrays 204, or the like. An offset stacked DRAM is next ~~place~~placed such that the offset half of the upper device in the stack rests on the initial discrete device or spacer 202 for support. Subsequent offset stacked devices are then placed, each upper device 208 resting on the lower of the stack previously placed for support, fully populating the module. The exposed half of the lower chip in the final offset stack place remains uncovered.